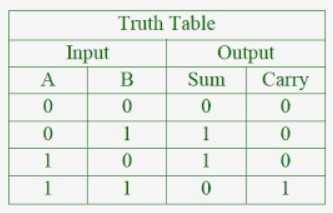
# HALF ADDER

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **EXP.NO: 21** | |  | | |
| **AIM:** | To design and implement the two bit half adder using | | Logisim | simulator. |

**PROCEDURE:**

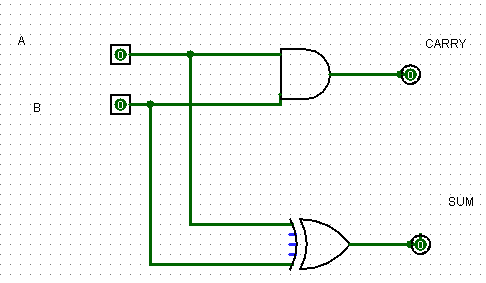
1. Pick and place the necessary gates.
2. Insert 2 inputs into the canvas.
3. Connect the inputs to the XOR gate and AND gate.
4. Insert 2 outputs into the canvas.
5. Make the connections using the connecting wires.6) Verify the truth table.

**TRUTH TABLE:**

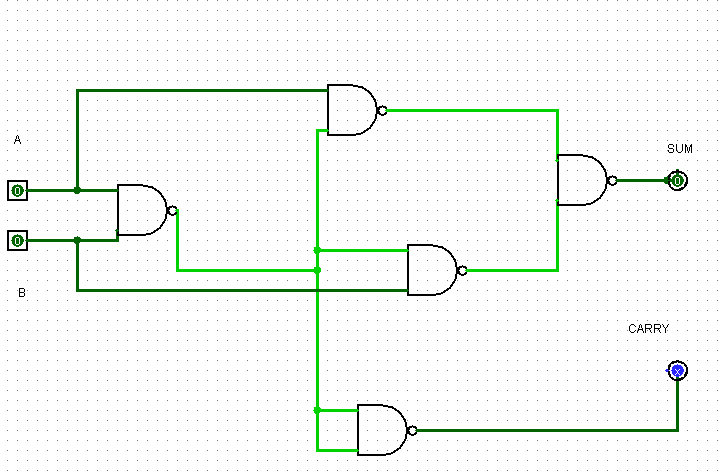


S = A XOR B C = A AND B

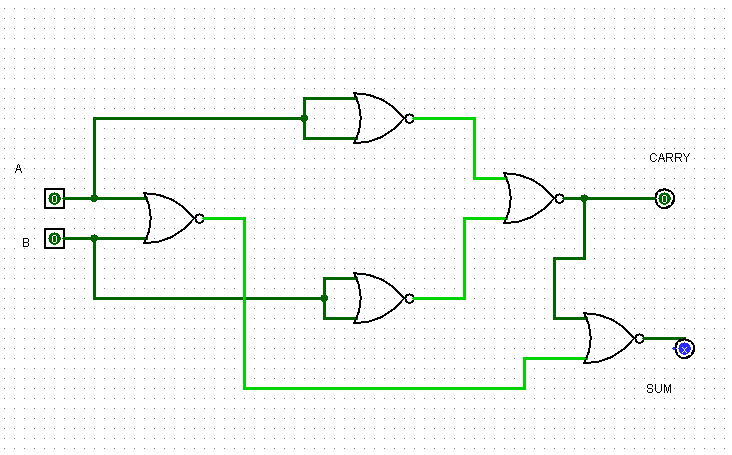
Logical Diagram:



Half Adder using NAND Gates:



|  |  |  |
| --- | --- | --- |
| Half Adder using | NOR | Gates: |



|  |  |  |  |
| --- | --- | --- | --- |
| **RESULT:** | | Thus 2-bit half adder has been designed and implemented successfully using | |
| logisim | simulator. | |  |